SHARCPAC™ Module Standard Promotes SHARC Multiprocessing

A four-way collaborative effort culminated in the module interface standard for multiprocessor systems based on Analog Devices ADSP-2106x SHARC digital signal processor. Already adopted by numerous third-party developers, the "SHARCPAC(tm)" standard resulted from contributions made by Ariel Corporation (Highland Park, NJ), Analog Devices (Norwood, MA), BittWare Research Systems (Concord, NH), and Ixthos Incorporated (Leesburg, VA).

With 480 MFLOPS delivered in only 13.95 square inches of space, SHARCPAC modules with four SHARCs deliver the industry's highest performance-per-area by a factor of three. Other SHARCPACs provide off-the-shelf processing, memory, and I/O device flexibility for multiprocessor system integrators.

"Embedded applications are constantly trying to pack more MFLOPS into less space," said leading DSP observer Will Strauss of Forward Concepts. "The SHARCPAC's improvement on this metric will be heartily welcomed by the industry."

The SHARCPAC standard is designed to provide modular, scalable integration for multiprocessor DSP designs. Commercially available SHARCPACs provide a fast way for developers to add DSPs, memory, and I/O to create custom systems using modules that are already established as stable and reliable circuit designs. The royalty-free open standard also allows developers to easily tailor system designs with custom-built SHARCPACs targeted at the functional requirements of particular applications.

SHARCPAC building-blocks give developers the easiest way to create custom multiprocessor SHARC systems using off-the-shelf modular components. At more than 34 MFLOPS-per-square-inch, SHARCPACs bring an incredible amount of processing power to the well-proven modular-design approach.

SHARCPAC modularity also allows designs to be quickly migrated between various host platforms such as ISA, PCI, and VME. System prototyping and early software development can be accomplished using the SHARCPAC site on the ISA-bus-based EZ-LAB® SHARC Development System from
Analog Devices.

Ariel Corp. launched the SHARCPAC module initiative with Analog Devices after realizing the dramatic performance-per-area achievable with a SHARC-based module. Ariel define the initial SHARCPAC specification and users' reference guide. Bittware Research Systems and Ixthos participated in finalizing the module specification.

BittWare and Alex Computer Systems of Ithaca, New York, were the first companies to market SHARCPAC modules, offering a half-a-dozen variations including single, dual and quad SHARCs, SRAM, and DRAM modules.

Now you can access the SHARCPAC specification on the World Wide Web.

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Module Specification

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- Analog Devices, Inc., Norwood, MA
- Ariel Corporation, Highland Park, NJ
- BittWare Research Systems, Inc., Concord, NH
- Ixthos Inc., Leesburg, VA

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1. INTRODUCTION

This document specifies the mechanical, electrical, and signal requirements for a SHARCPAC™ module. It is intended to provide the system designer all the information necessary to construct a SHARCPAC module or a SHARCPAC-compatible module site on a host system board. A list of manufacturers that provide SHARCPAC-related components and services is presented in section 6.

This section contains a complete overview of the SHARCPAC module, including a discussion of required and optional features, and theory of operation. A list of literature relevant to this specification is located at the end of this section.

1.1 SHARCPAC OVERVIEW

A SHARCPAC Module is a compact, modular solution to satisfy the need within the signal processing community for multiple processors, high speed, and high density of memory and I/O capability. By offering a standardized, straightforward, and flexible design, system designers can concentrate on integration and system-specific issues rather than core DSP/memory design. Modularity also brings the flexibility of upgrading processor types and speeds and memory with little impact on system hardware design.

SHARCPAC Modules were conceived with Analog Devices' ADSP-2106x Super Harvard ARchitecture Computer (SHARC™) as the processor of choice. The SHARC product family offers a variety of high-performance processors with the following features:

- ADSP-21020 compatible processor core, providing up to 40 MIPS sustained and up to 120 MFLOPS peak.
- Up to 4 Megabits of zero wait-state, dual-ported, internal SRAM.
- Three independent internal busses allowing a maximum internal data transfer rate of over 500 Mbytes per second.
- Six communications ports providing direct SHARC to SHARC communication capabilities.
- Two synchronous serial ports providing word lengths up to 32 bits, programmable 'on the fly' A-law or µ-law companding, and multichannel modes for TDM interfaces.
- 10-channel DMA controller that can be used by link ports, external ports, and the serial ports.
- Intelligent bus interface allowing multiple SHARCs to share the same system bus without external arbitration or buffer logic.

The SHARCPAC Module is designed to cover a wide range of DSP requirements, without burdening users with extra unused features or tradeoffs. Modules can have multiple processors, external memory devices, and custom I/O circuitry. Host system boards can be designed with multiple SHARCPAC Module sites and modules with different capabilities can be installed to create a custom system. The SHARC processor's external system bus is included in the SHARCPAC interface connector to allow direct interprocessor communication and shared memory devices between SHARCPAC resources and system board resources.

1.2 ADDITIONAL LITERATURE

In addition to this specification, the reader is referred to the following publications:

- *ADSP-2106x SHARC User's Manual*, available from Analog Devices
- *ADSP-21060/62 SHARC Data Sheet*, available from Analog Devices
- *NM93C46AL 1024-Bit Serial EEPROM Data Sheet*, available from National Semiconductor

2. SHARCPAC MODULE ARCHITECTURE

The SHARCPAC module can accommodate many different processor and memory device configurations. Its 3.1 × 4.5 inch size allows sufficient space to mount up to four SHARC processors on a single side and surface mount components can be mounted on both sides of the module (please note the restrictions given in the section entitled *Mechanical Specifications*); however, certain characteristics of the module connector interface will influence the architecture of the module.

2.1 OVERVIEW

The primary use for a SHARCPAC module is to provide SHARC processors that can be accessed by the host system. For this reason, the interface contains all of the external SHARC signals required for multiprocessor connections. SHARC processors on a SHARCPAC module can connect to a cluster of SHARC processors on the host system or on other SHARCPAC modules (up to 6 processors total per cluster) which allows direct memory access through the SHARC external bus (see Figure 2-1). In addition, SHARC link ports, serial ports, flags, and interrupts provide alternate paths for communication and signaling.

Memory banks can be accessed through the SHARC external bus, making it accessible to all SHARC processors in a cluster. The SHARCPAC interface supports up to four memory select signals. Input / output devices may be memory-mapped, connected directly to link ports or serial ports for data exchange.

Modules can be configured and identified through the Module Control Interface. This interface has an 8-bit data interface separate from the SHARC external bus that is accessible to the host system.

The following sections describe each of the SHARCPAC features in more detail.

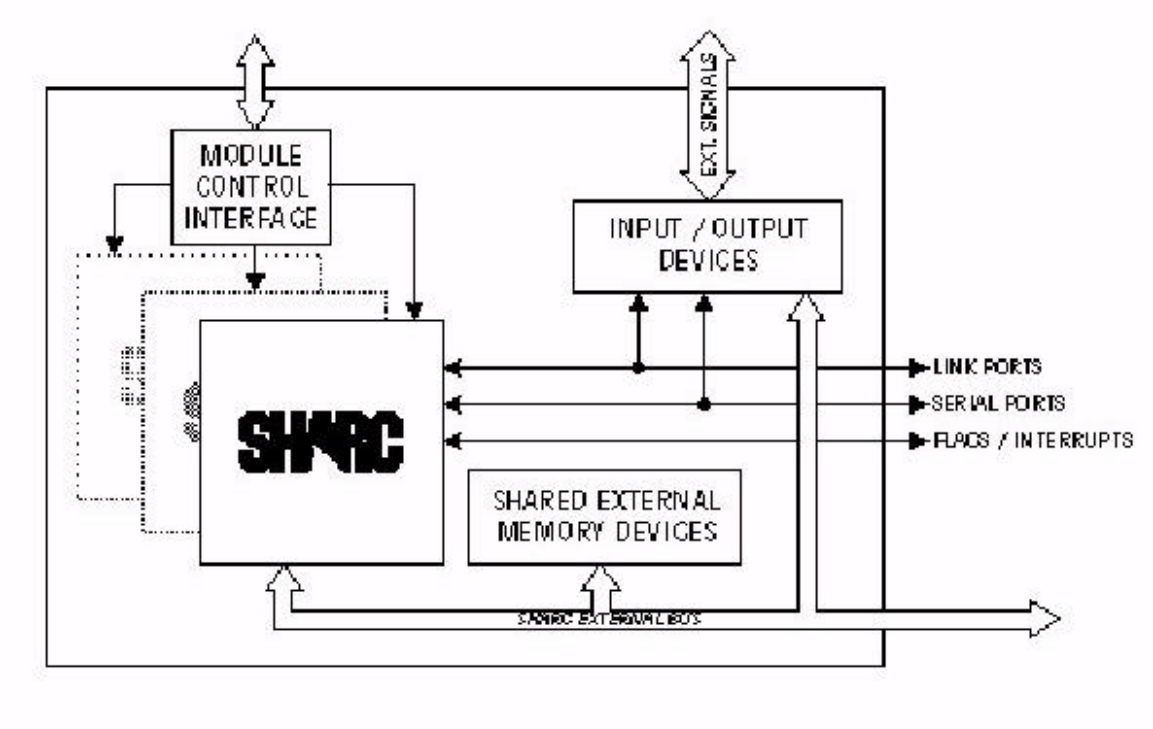

Figure 2-1 – SHARCPAC Module Architecture

2.2 SHARC EXTERNAL BUS

The SHARC external bus is the primary method for accessing SHARC processors. It supports the full 32 address bits and 48 data bits offered by the SHARC processor. It provides access to other SHARC processors connected with the SHARC processor's built-in bus master arbitration. Host system processors that do not have bus-master capability can control the bus with the Host Bus Request (HBR) and Host Bus Grant (HBG) signals. Up to six SHARC processors can be selected by these processors using individual chip-select signals. Memory-mapped devices can be selected by the four memory select signals.

2.2.1 Multiprocessor ID Assignment

The SHARC multiprocessor model defines clusters of up to six processors that share a single external bus. Individual SHARC processors are arbitrated and given access based on their multiprocessor identification (MID) number, which is defined by the ID_{2-0} pins on the SHARC. Valid MID numbers in a multiprocessor cluster range from 1 to 6. In order to avoid conflicting MID numbers, SHARCPAC modules should provide a method for configuring these numbers for each processor that is connected to the SHARC external bus on the SHARCPAC interface. This can be accomplished with jumpers on the module or with register bits in the Module Control Interface. When default MID numbers are assigned to SHARCPAC module processors by the designer, the recommended starting number is 6; the recommended starting number for SHARC processors on host system boards is 1. The reduces the likelihood of having to reconfigure a SHARCPAC module before a system can be started.

2.2.2 DMA Handshaking

A single set of DMA handshaking signals (DMAR / DMAG) is available on the SHARCPAC interface. The signals can be connected directly to the handshaking lines of one of a SHARC processor's two DMA channels.

2.3 LINKS

The SHARCPAC interface supports up to 16 off-module links. For purposes of generality they are named L00 - L15. If less than 16 links go off-module, use of the lower numbered link ports is recommended. Link number zero (L00) must always be connected to the primary SHARC processor's link port 4 to support link booting.

2.4 SERIAL PORTS

The four serial ports available in the SHARCPAC interface are named SP0 - SP3. They allow full-duplex connections consisting of separate data, frame sync, and clock signals for receive and transmit paths.

2.5 INTERRUPTS

Up to eight interrupt signals from the host system can be connected to SHARC processors on a SHARCPAC module. No special assignments are required, however use of lower-numbered interrupt signals is recommended.

2.6 PROCESSOR FLAGS

Up to eight processor flag signals are available for passing status to and from the host system. Although these signals are bi-directional when connected to the SHARC processor's flag pins, they may be connected to devices that are dedicated as inputs or outputs. Input-only devices on SHARCPAC modules (or output-only devices on the host system) should use flag signals 0 - 3. Output-only devices on SHARCPAC modules (or input-only devices on the host system) should use flag signals 4 - 7.

2.7 JTAG EMULATION

The SHARCPAC interface supports the standard SHARC in-circuit emulation signals. A JTAG scan path that originates on the host system board can be routed through devices on the SHARCPAC module and then routed back to the host board.

2.8 MODULE CONTROL INTERFACE

The Module Control Interface (MCI) provides a method for configuring a module and for providing status and configuration information to the host system. It is accessed by the host system through a separate 8-bit data bus. The MCI is optional on SHARCPAC modules; however, it is *strongly recommended* that a module implements an MCI. The carrier board is required to support the MCI to ensure compatibility with SHARCPAC modules that need configuration before they can operate.

Four address bits define 16 ports / registers; seven of the ports have reserved functionality as defined by this specification. The remaining ports can be defined by the module designer. Table 2-1 shows the addresses of the ports that are defined by this specification.

Table 2-1 – MCI Address Map

Address	Register / Port
0x0	Reset Register
0x1	Boot Configuration Register
0x2	ID EEPROM Access Port
0x3	MID Configuration Register
0x4	Status Register
0x5	Interrupt Mask Register
0x6	Interrupt Generate Port
0x7 - 0xF	Optional / Module Specific

The individual registers are described in detail below. When a register refers to control or status information for multiple SHARC processors (up to eight), individual SHARC processors are named “A” through “H”. SHARC A should designate the primary SHARC processor on the module.

2.8.1 Reset Register

7	6	5	4	3	2	1	0
RSTH	RSTG	RSTF	RSTE	RSTD	RSTC	RSTB	RSTA

Each bit in this register is connected to the respective SHARC processor’s reset pin. Writing a zero brings the processor into reset, while a one takes it out of reset. The outputs of this register should be logically combined with the Master Reset (MR) signal so that when the host system asserts MR, all module processors are reset.

2.8.2 Boot Configuration Register

7	6	5	4	3	2	1	0
BMH	BMG	BMF	BME	BMD	BMC	BMB	—

The Boot Configuration register sets the boot mode of the secondary SHARC processors. The boot mode of the primary SHARC processor is programmed with the B0-B1 pins (see 2.1, *System Control Signals*). The following table defines the boot modes for secondary SHARC processors.

Bit	DSP B-H Boot Mode
0	Link booting
1	Host booting

2.8.3 ID EEPROM Access Port

7	6	5	4	3	2	1	0
—	—	—	—	EEDO	EEDI	EESK	EECS

EECS *(Write-only)* Chip Select
EESK *(Write-only)* Serial Data Clock
EEDI *(Write-only)* Serial Data Input (to EEPROM)
EEDO *(Read-only)* Serial Data Output (from EEPROM)

These register bits are connected directly to the serial EEPROM.

2.8.4 MID Configuration Register

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

These register bits should be used to configure the multiprocessor identification (MID) pins on each SHARC processor. Specific register bit definitions and MID assignment schemes can be defined by the module designer.

2.8.5 Status Register

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

These register bits should be used to provide real-time status of the module. Specific register bit definitions can be defined by the module designer.

2.8.6 Interrupt Mask Register

7	6	5	4	3	2	1	0
IRQH	IRQG	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA

These register bits define a mask that controls which processors are interrupted when the host system accesses the Interrupt Generate Port. A zero will prevent (mask) the interrupt, while a one will allow the interrupt to be generated.

2.8.7 Interrupt Generate Port

A write to this port causes an interrupt to occur on each of the SHARC processors that are selected in the Interrupt Mask Register. The recommended interrupt pin that should be used on each processor is IRQ0.

2.8.8 Optional Registers

Optional registers are not controlled by this specification. They may be defined by a particular module for any purpose.

2.9 ID EEPROM

The ID EEPROM contains module identification and configuration information. The host system can read this information to make a run time determination of the system profile or to perform module-level testing. It should be a serial EEPROM, compatible with the National Semiconductor part number NM93C46AL. It is accessed through the MCI.

2.10 MISCELLANEOUS CONTROL FEATURES

The following sections describe the remaining control features of the SHARCPAC interface.

2.10.1 Module Reset

This signal allows the host system to return the SHARCPAC module to its power-up state.

2.10.2 Boot Mode Control

The SHARCPAC interface has two pins (B0 - B1) that are programmed by the host system to control the booting method of the primary SHARC processor (at a minimum). These pins should be programmed prior to releasing the Module Reset signal.

2.10.3 SHARC Sense

This signal provides a method for SHARCPAC modules to indicate to the host system that at least one SHARC processor is present on the module. The host can detect the state of this signal to change hardware configuration settings. For example, it may redefine MID numbers or reroute the JTAG scan path.

2.10.4 Timer Expiration

This signal can be used by the SHARCPAC module to provide a general purpose periodic signal to the host system. It is usually connected to the TIMEXP output of a SHARC processor on the module.

2.11 REQUIRED / OPTIONAL FEATURES

Table 2-2 lists the major features described in this chapter and whether or not they are required for SHARCPAC module compatibility.

Table 2-2 – Required / Optional SHARCPAC Features

Feature	Module	Host Site
Module Control Interface	• Optional	• Required
SHARC external bus	• Not required for modules that do not have memory-mapped devices.	• Optional
Link Ports	• Primary SHARC must have capability of booting from SHARCPAC link 0. • Primary SHARC must be able to boot remaining SHARC processors.	• Must support booting a SHARC connected to SHARCPAC link 0.
Serial Ports	• Optional	• Optional
Processor Flags	• Optional	• Optional
Interrupts	• Optional	• Optional
JTAG signals	• At a minimum, must route TDI to TDO if SENSE is active.	• Optional
Boot Mode Signals	• Optional	• Required
Module Reset	• Required	• Required
SHARC Sense	• Optional	• Optional
Timer Expiration	• Optional	• Optional

3. SOFTWARE CONSIDERATIONS

This section contains information related to software development for the SHARCPAC module. Issues that are discussed cover resetting the module, the different booting modes, accessing the Module Control Interface, and programming the ID EEPROM.

3.1 MODULE RESET

The SHARCPAC module is placed in reset by asserting the MR (module reset) signal. This immediately halts all SHARC processors and places them in their reset state. The programmer should ensure that the Boot Mode Control signals (B0 - B1) are programmed to the desired values before releasing the MR signal.

3.2 BOOTING

The Boot Mode Control pins (B0 - B1) set the boot mode for the primary SHARC processor when it comes out of reset. Table 3-1 lists the boot modes defined by the Boot Mode Control pins. Each boot mode is described in the following sections. More detailed information is in the *ADSP-2106x SHARC User's Manual.*

Table 3-1 – Primary SHARC Processor Boot Modes

B1	B0	SHARC A Boot Mode
0	0	Link booting
0	1	Host booting
1	0	PROM (if available)
1	1	No booting (execute from external memory)

3.2.1 Link Booting

When this mode is selected, the SHARC processor will wait for boot data to arrive at its Link 4. Since the primary SHARC processor's Link 4 is always tied to the SHARCPAC interface's Link 0, the host system must provide the bootstrap data via this link port.

3.2.2 Host Booting

When this mode is selected, the SHARC processor will wait for 16-bit boot data to arrive from external port buffer zero (EPB0). The host system must provide the boot code through the SHARC processor's external data bus.

3.2.3 PROM Booting

When this mode is selected, the SHARC processor's BMS pin becomes an output to be used as a chip select for an 8-bit EPROM. It will automatically load the bootstrap code from the EPROM.

3.2.4 No Booting

When this mode is selected, the SHARC processor will start executing instructions from address 0x0040 0004 in external memory (bank 0).

3.3 ID EEPROM MEMORY MAP

The ID EEPROM contains module identification and configuration information. It is a 1024-bit device organized into 64 words that are 16 bits wideTable 3-2 lists the information that is stored in the EEPROM and the following sections describe the data in detail.

Table 3-2 – ID EEPROM Data Format

Location	Definition
0	MCI Magic Number (0xBEEF)
1 - 2	Module Serial Number
3	PCB Revision Number
4	ECO Revision Level
5	Number of ECOs performed at this level
6 - 8	Factory check date
9	Vendor Code
10	Vendor Product ID
11	SHARCPAC Revision
12	Number of SHARC processors on module
13 - 14	Processor Descriptors
15 - 18	Memory Bank Descriptors
19 - 26	Link Descriptors
27	Flag / IRQ Descriptor
28-39	Module Specific
40	EEPROM Checksum
41 - 63	User Definable bits

3.3.1 MCI Magic Number

This location is always programmed to 0xBEEF. Reading 0xBEEF from this location indicates that the EEPROM is programmed and contains valid information.

3.3.2 Module Serial Number

These two locations contain the 32-bit module serial number. This number is defined by the module manufacturer. Location 1 should contain the most significant 16 bits and location 2 should contain the least significant 16 bits.

3.3.3 PCB Revision Number

The Printed Circuit Board revision number: 0 = A, 1 = B, 2 = C, etc.

3.3.4 ECO Revision Level

Engineering Change Order revision level. Indicates the level of ECO modifications to the PCB.

3.3.5 Number of ECOs performed at this level

Engineering Change Order minor level. Indicates the number of ECOs performed at the level described in the ECO Revision Level.

3.3.6 Factory Check Date

These three locations contain the date that the module was tested at the factory. It is assumed that the ID EEPROM will be programmed during factory test. The following table describes the contents of each location.

Location	Contents	Format / Range
6	Day of month	1 - 31
7	Month	1 - 12
8	Year	0 - 9999

3.3.7 Vendor Code

This 16-bit value identifies the manufacturer of the module. Unique vendor codes are maintained and assigned by Analog Devices (see section 6, *List of Manufacturers*).

3.3.8 Vendor Product ID

This 16-bit value identifies a particular module within a vendor's own product line. It may specify a module family or a specific assembly of a module. These ID numbers are maintained and assigned by the manufacturer of the module.

3.3.9 SHARCPAC Revision

This specifies the *minimum* revision level of this SHARCPAC module specification that is required to be supported by the carrier board to operate properly with this module. The most significant 8 bits represents the major revision number; the least significant 8 bits represents the minor revision number. For example, revision 1.2 would be represented by the value 0x0102.

3.3.10 Number of SHARC processors

The number of ADSP-2106x SHARC processors installed on the module. This value can range from 0 to 8.

3.3.11 Processor Descriptors

These two locations describe up to eight SHARC processors that are installed on the module. Each location contains four 4-bit codes that identify the processor type and speed of a single processor.

Location	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
13	SHARC D	SHARC C	SHARC B	SHARC A
14	SHARC H	SHARC G	SHARC F	SHARC E

Code	Processor type and speed
0000	33 MHz ADSP-21062
0001	40 MHz ADSP-21062
0010	33 MHz ADSP-21060
0011	40 MHz ADSP-21060
All others	*Reserved for future use.*

3.3.12 Memory Bank Descriptors

These four locations describe up to four memory banks that are installed on the module. The four memory banks are selected by the $\overline{MS}_{3-0}$ signals. Each location contains a 16-bit code that identifies the properties of a memory bank. The following table shows the bit fields:

Location	Bank	15	14	13 12	11 10 9	8 7 6 5	4 3 2	1 0
15	0	—	R	WT_MODE	WAIT_STATES	DEPTH	WIDTH	TYPE
16	1	—	R	WT_MODE	WAIT_STATES	DEPTH	WIDTH	TYPE
17	2	—	R	WT_MODE	WAIT_STATES	DEPTH	WIDTH	TYPE
18	3	—	R	WT_MODE	WAIT_STATES	DEPTH	WIDTH	TYPE

Where the fields are defined as follows:

Field	Description
TYPE	Memory type: 00 = None, 01 = SRAM, 10 = DRAM, 11 = Other
WIDTH	The width of the memory bank in bytes.
DEPTH	The depth of the memory is defined the same as the MSIZE field in the SHARC processor's SYSCON register, which can be described by: $\log_2$(bank size) - 13
WAIT_STATES	The number of wait states required for access by the SHARC processor (see table below). This number is defined the same as the EBxWS field in the SHARC processor's WAIT register.
WT_MODE	The wait state mode required for access by the SHARC processor (see table below). This number is defined the same as the EMxWM field in the SHARC processor's WAIT register.
R	Indicates whether the memory bank is fixed at the default memory select or if it is relocatable. 0 = Fixed, 1 = Relocatable

The WAIT_STATES field has the following definitions:

WAIT_STATES	# of Wait States	Bus Idle Cycle?	Hold Time Cycle?
000	0	no	no
001	1	yes	no
010	2	yes	no
011	3	yes	no
100	4	no	yes
101	5	no	yes
110	6	no	yes
111	0	yes	no

The WT_MODE field has the following definitions:

WT_MODE	Wait State Mode
00	External acknowledge only (ACK)
01	Internal wait states only
10	Both internal and external acknowledge required
11	Either internal or external acknowledge sufficient

3.3.13 Link Descriptors

These eight locations describe up to sixteen links from the SHARCPAC module interface that may be connected to SHARC processors on the module. Each location describes the destination SHARC processor and link number for two SHARCPAC links.

Location	15 14 13 12	11	10 9 8	7 6 5 4	3	2 1 0
19	Link 1⇔Proc. #	—	Link 1⇔Link #	Link 0⇔Proc. #	—	Link 0⇔Link #
20	Link 3⇔Proc. #	—	Link 3⇔Link #	Link 2⇔Proc. #	—	Link 2⇔Link #
21	Link 5⇔Proc. #	—	Link 5⇔Link #	Link 4⇔Proc. #	—	Link 4⇔Link #
22	Link 7⇔Proc. #	—	Link 7⇔Link #	Link 6⇔Proc. #	—	Link 6⇔Link #
23	Link 9⇔Proc. #	—	Link 9⇔Link #	Link 8⇔Proc. #	—	Link 8⇔Link #
24	Link 11⇔Proc. #	—	Link 11⇔Link #	Link 10⇔Proc. #	—	Link 10⇔Link #
25	Link 13⇔Proc. #	—	Link 13⇔Link #	Link 12⇔Proc. #	—	Link 12⇔Link #
26	Link 15⇔Proc. #	—	Link 15⇔Link #	Link 14⇔Proc. #	—	Link 14⇔Link #

Where the fields are defined as follows:

Link *x* ⇔ Proc. # This is the processor number to which Link*x* from the SHARCPAC interface connects. It can range from 0 to 7 (representing SHARC processors “A” to “H”).

Link *x* ⇔ Link # This is the link number on the processor specified above to which Link*x* from the SHARCPAC interface connects. It can range from 0 to 5.

3.3.14 Flag / IRQ Descriptor

This value describes the SHARCPAC module’s use of the interrupt and flag signals. A zero indicates that the resource not used; a one indicates that the resource is connected to a device on the module.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F7	F6	F5	F4	F3	F2	F1	F0	I7	I6	I5	I4	I3	I2	I1	I0

3.3.15 EEPROM Checksum

This number is used to verify the contents of the ID EEPROM. It is calculated from the sum of all of the programmed values in locations 0 to 39, modulo 65536.

4. ELECTRICAL SPECIFICATIONS

This section specifies all of the electrical parameters necessary to properly interface to a SHARCPAC module. The SHARCPAC interface requires 360 signals for proper implementation. The various signal types and electrical characteristics of each type is described below.

4.1 SIGNAL TYPE DEFINITION

Each signal is described in the following manner:

NAME	Active State	Signal Type

Description of the signal.

NAME is simply the name of the signal. Multiple signals with numbered name schemes are represented by the first name and the last name with a hyphen as a separator. For example, there are four independent signals HA0, HA1, HA2, HA3; however, they are named as HA0 - HA3.

Active State is one of the following:

Table 4-1 – Active State Descriptions for SHARCPAC Signals

Active State	**Description**
Active High	Indicates that the active state of the signal is represented by a nominal voltage level of +5 Volts.
Active Low	Indicates that the active state of the signal is represented by a nominal voltage level of 0 Volts.
Falling Edge Triggered	Indicates that the active state of the signal is the +5 Volt to 0 Volt transition or edge.
Rising Edge Triggered	Indicates that the active state of the signal is the 0 Volt to +5 Volt transition or edge.

The Signal Type is one of the following:

Table 4-2 – Signal Type Descriptions of the SHARCPAC Module Signals

Signal Type	**Description**
Input	Indicates that the signal is an input to the SHARCPAC module.
Output	Indicates that the signal is driven by the SHARCPAC module.
Bi-directional	Indicates that the signal is both an input to and an output from the SHARCPAC module.
Power/Ground	Indicates that these signals provide power and ground references to the SHARCPAC module.

4.2 PIN FUNCTIONAL GROUPS

This section describes the various signals for the full implementation of the SHARCPAC module. These signals can be divided into eight categories: system control, external bus, links, serial ports, flags, interrupts, JTAG emulation/control, and power/ground. *All signals are described with respect to the SHARCPAC module.*

The following table summarizes the pin count of a SHARCPAC module, organized by functional group.

Table 4-3 – SHARCPAC Pin Count by Functional Group

Description	Total Signals
System Control	32
External Bus Data (48 bits)	48
External Bus Address (32 bits)	32
External Bus Control	28
Link Ports (16)	96
Serial Ports (4)	24
Flags (8)	8
Interrupts (8)	8
JTAG	7
Power/Ground	65
User Defined	8
RESERVED	4
TOTAL	**360**

4.2.1 System Control Signals

B0 – B1	Active High	Input

These signals are used to place the module in one of four known states following a module reset to control the boot mode of the primary SHARC processor.

CLKINA – CLKINC	Active High	Input

These are the 33 or 40 MHz master clock signals used by the 2106x processors and the module resources. Further information is described in section 4.3, *Clock Distribution and Termination*.

HA0 – HA3	Active High	Input

Four address lines to uniquely address the host interface's sixteen MCI registers / ports.

HD0 – HD7	Active High	Bi-directional

Eight bi-directional data lines used to exchange data with the host system. These signals should tristate or switch to inputs when HSEL is not active.

HPROG0 – HPROG7	Active High	Bi-directional

These eight signals are used for internal test and configuration, typically for FPGA programming. The recommended connector on the host system is an eight-pin, single-row, strip header (0.1 in. spacing).

HRD	Active Low	Input

HRD is the host read strobe and is used to indicate to the SHARCPAC module that the host system is reading one of the sixteen MCI registers / ports.

HSEL	Active Low	Input

This is the Host Select signal. The host must assert this signal to select the MCI registers / ports for reading or writing.

HWR	Rising Edge Triggered	Input

HWR is the host write strobe and is used to indicate to the SHARCPAC module that the host system is writing to one of the sixteen MCI registers / ports.

MR	Active Low	Input

The MR signal is used to place the SHARCPAC module in the reset state. When active, this signal forces all 2106x processors into the reset state, initializes any on-board controller logic, and initializes all control registers to their default values.

SENSE	Active Low	Input

The SENSE signal indicates the presence of a SHARC processor on the SHARCPAC module. If a SHARC processor is present, the SHARCPAC module should unconditionally ground this signal. In this case, the SHARCPAC module must ensure that the JTAG signal TDI connects to TDO (either directly or through JTAG devices), since the host system may route the JTAG scan path to the module when SENSE is active. SHARCPAC modules that do not have a SHARC processor (e.g., memory expansion modules) can leave this signal unconnected. The host system must pull this signal high via a 10 kΩ resistor.

TIMEXP	Active High	Output

This is the timer expired signal. It should be tied to the TIMEXP pin on the module's primary SHARC processor.

4.2.2 Link Signals

The SHARCPAC module interface implements sixteen complete links ports named L00 – L15. Each link port consists of six signals with identical functionality on each port: L*xx*ACK, L*xx*CLK, and L*xx*DAT0 – L*xx*DAT3. Each of these signals should be series terminated near the SHARC processor's pins with 39 Ω resistors. This applies to processors on modules as well as the host system board.

L*xx*ACK	Active High	Bi-directional

This is the acknowledge signal for link port number *xx*.

L*xx*CLK	Active High	Bi-directional

This is the clock signal for link port number *xx*.

L*xx*DAT0 – L*xx*DAT3	Active High	Bi-directional

These signals are the four bi-directional data bits for link port number *xx*.

4.2.3 Serial Port Signals

The SHARCPAC module interface implements four serial ports named SP0 – SP3. Each serial port consists of six signals with identical functionality on each port: SP*x*DR, SP*x*DT, SP*x*RCLK, SP*x*RFS, SP*x*TCLK, and SP*x*TFS. Each of these signals should be series terminated near the SHARC processor's pins with 39 Ω resistors. This applies to processors on modules as well as the host system board.

SP*x*DR	Active High	Input

This is the data receive signal of serial port number *x*.

SP*x*DT	Active High	Output

This is the data transmit signal of serial port number *x*.

SP*x*RCLK	Active High	Bi-directional

This is the receive clock signal of serial port number *x*.

SP*x*RFS	Active High	Bi-directional

This is the receive frame sync signal of serial port number *x*.

SP*x*TCLK	Active High	Bi-directional

This is the transmit clock signal of serial port number *x*.

SP*x*TFS	Active High	Bi-directional

This is the transmit frame sync signal of serial port number *x*.

4.2.4 Flag Signals

FLAG0 – FLAG7	Active High	Bi-directional

These signals are connected directly to the 2106x processors' flag pins. Refer to section 2.6, *Processor Flags* for information regarding the connection of these signals to unidirectional devices.

4.2.5 Interrupt Signals

IRQ0 – IRQ7	Active Low or Falling Edge Triggered	Input

These signals are connected directly to the interrupt request pins on the SHARCPAC module's processors. Unused interrupt signals must be pulled high on the carrier board to prevent unintentional interrupts.

4.2.6 JTAG Emulation Signals

EMU	Active Low	Output

This is the JTAG emulation status signal.

ICSA	Active Low	Output

This is the JTAG in-circuit signal analysis signal. Its use is currently reserved and should not be connected to any devices.

TCK	Active High	Input

This is the JTAG scan test clock signal that is generated by the host system and connected to all of the JTAG compatible devices on the SHARCPAC module that will participate in the JTAG boundary scan path.

TDI	Active High	Input

This is the JTAG test data input signal which receives the boundary scan serial data. It should be connected to the first JTAG compatible device on the SHARCPAC module that will participate in the JTAG boundary scan path. If no devices on the SHARCPAC module participate in the JTAG path, this signal should be connected directly to TDO.

TDO	Active High	Output

This is the JTAG test data output signal which outputs the serial data from the last SHARCPAC module device that is connected to the JTAG boundary scan path.

TMS	Active Low	Input

This is the JTAG test mode select signal. It should be connected to all of the JTAG compatible devices on the SHARCPAC module that will participate in the JTAG boundary scan path.

TRST	Active Low	Input

This is the JTAG test reset signal that is generated by the host system and connected to all of the JTAG compatible devices on the SHARCPAC module that will participate in the JTAG boundary scan path.

4.2.7 External Bus Signals

The SHARCPAC module interface supports the following external bus signals to allow the host system direct access to external memory-mapped devices and the multiprocessor memory space of 2106x processors on the module. These signals can be directly connected to all devices in a shared cluster.

ACK	Active High	Bi-directional

This is the memory acknowledge signal.

ADDR00 – ADDR31	Active High	Bi-directional

These are the thirty-two bus address signals.

ADRCLK	Active High	Bi-directional

This is the Address Clock signal for synchronous external memories.

BMS	Active Low	Bi-directional

This is the Boot Memory Select signal.

BR1 – BR6	Active Low	Bi-directional

These are the six Multiprocessing Bus Request signals.

CPA	Active Low	Bi-directional

This is the Core Priority Access signal.

CS0 – CS5	Active Low	Input

These are the six Chip Select signals that allow the host processor to select an 2106x processor.

DATA00 – DATA47	Active High	Bi-directional

These are the forty-eight bus data signals.

DMAG	Active Low	Bi-directional

This is the Direct Memory Access (DMA) Grant signal. It should be connected to the DMAG1* pin on all SHARC processors that are connected to the external bus.

DMAR	Active Low	Bi-directional

This is the DMA Request signal. It should be connected to the DMAR1* pin on all SHARC processors that are connected to the external bus.

HBG	Active Low	Bi-directional

This is the Host Bus Grant signal.

HBR	Active Low	Bi-directional

This is the Host Bus Request signal.

MS0 – MS3	Active Low	Bi-directional

These are the four external memory bank select signals.

PAGE	Active High	Bi-directional

This is the DRAM page boundary signal.

RD	Active Low	Bi-directional

This is the memory read strobe signal.

REDY	Active High	Bi-directional

This is the Host Bus Acknowledge signal.

RPBA	Active High	Bi-directional

This is the Rotating Priority Bus Arbitration Select signal.

SBTS	Active Low	Bi-directional

This is the Suspend Bus Tristate signal.

SW	Active Low	Bi-directional

This is the synchronous write select signal.

WR	Active Low	Bi-directional

This is the memory write strobe signal.

4.2.8 Power/Ground Signals

VDD	Power

These twenty signals supply the external power (nominally +5.0 V_{DC} or +3.3 V_{DC}) for the devices on the SHARCPAC module.

GND	Ground

These forty-five signals provide the external power supply return for the devices powered by the VDD signals.

4.3 CLOCK DISTRIBUTION AND TERMINATION

A SHARCPAC module is provided with three clock lines that are driven by the host carrier board. All three lines should be driven independently and exactly in phase with the same clock signal that drives SHARC processors on the carrier board. Multiprocessor SHARC designs require clock skew of <1nS. To minimize skew between SHARC processors, the following rules should be adhered to:

1. Minimize clock trace length. Long traces increase delay to clock loads on that trace. This can lead to skew problems. Keep traces under six inches. Traces on the carrier board to the SHARCPAC interface should be especially short since the SHARCPAC module will have additional trace length on it.
2. Each clock trace should be end-terminated. The recommended termination is a series combination of a 50Ω resistor and a capacitor that brings the total load to 50pF.
3. Consider using an adjustable skew clock driver.

4.4 5V VS. 3.3V

Since only one voltage is supplied to the SHARCPAC module, all of the components on a module should operate at the same voltage level as the SHARC processor.

4.5 AC TIMING CHARACTERISTICS

The following sections detail the AC timing parameters for SHARCPAC module interfaces. Please note that read and write timing are compatible with a 40 MHz SHARC processor operating with one wait state.

4.5.1 Reset Timing

Figure 4-1 and Table 4-4 describe the timing parameters for the Master Reset (MR) signal and the Boot Mode Control (B0 - B1) signals.

Table 4-4 – Master Reset (MR) Timing Parameters

Name	Description	Min	Max	Unit
tRP	MR* pulse width	150	-	ns
tBS	B0/B1 setup to MR* inactive	50	-	ns

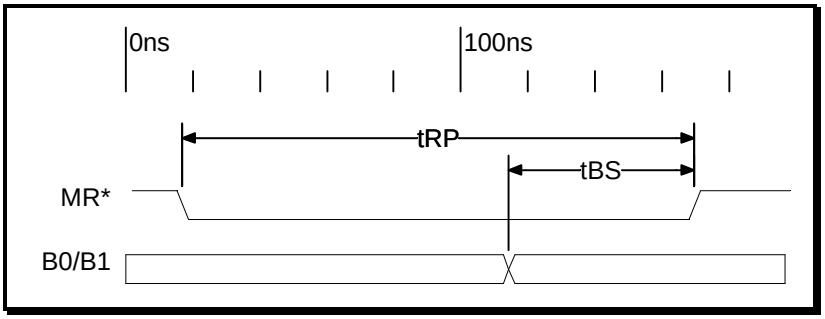

Figure 4-1 – Master Reset (MR) Timing Diagram

4.5.2 MCI Read Timing

Figure 4-2 and Table 4-5 describe the timing parameters for the host system when it reads from the Module Control Interface.

Table 4-5 – MCI Read Timing Parameters

Name	Description	Min	Max	Unit
tAS	Address setup to HSEL* active	0	-	ns
tAR	Address setup to HRD* active	2	-	ns
tAH	Address hold from HRD* inactive	0	-	ns
tSR	HSEL* active to HRD* active	2	-	ns
tRP	HRD* pulse width	35	-	ns
tDA	Data access time from HRD* active	-	30	ns
tDH	Data hold time from HRD* inactive	0	-	ns

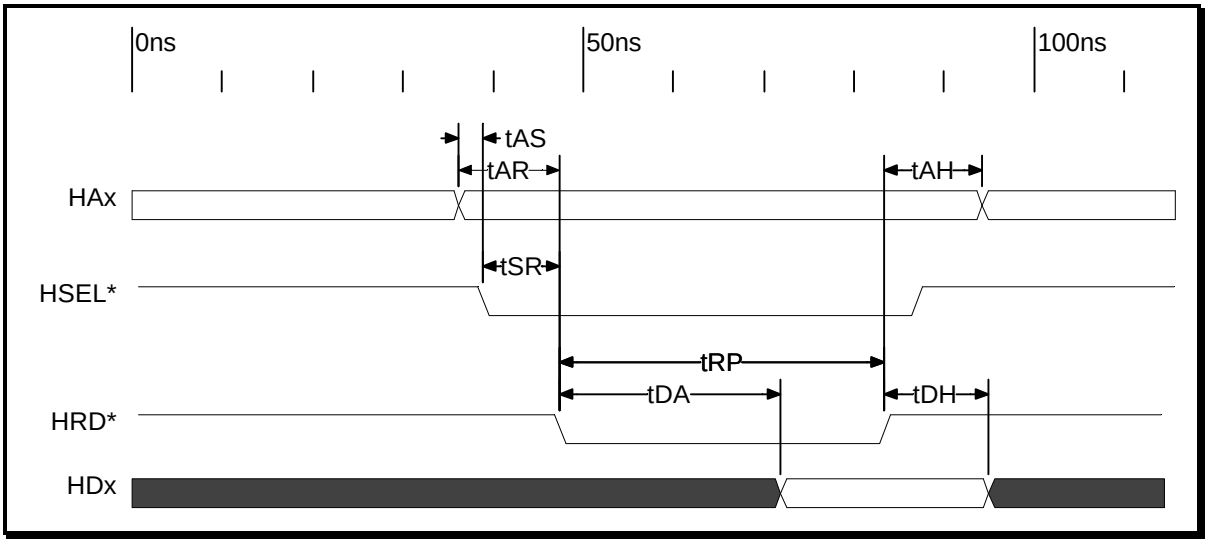

Figure 4-2 – MCI Read Timing Diagram

4.5.3 MCI Write Timing

Figure 4-3 and Table 4-6 describe the timing parameters for the host system when it writes to the Module Control Interface.

Table 4-6 – MCI Write Timing Parameters

Name	Description	Min	Max	Unit
tAS	Address setup to HSEL* active	0	-	ns
tAR	Address setup to HWR* active	3	-	ns
tAH	Address hold from HWR* inactive	0	-	ns
tSW	HSEL* active to HWR* active	3	-	ns
tWP	HWR* pulse width	35	-	ns
tDS	Data setup time to HWR* inactive	30	-	ns
tDH	Data hold time from HWR* inactive	0	-	ns

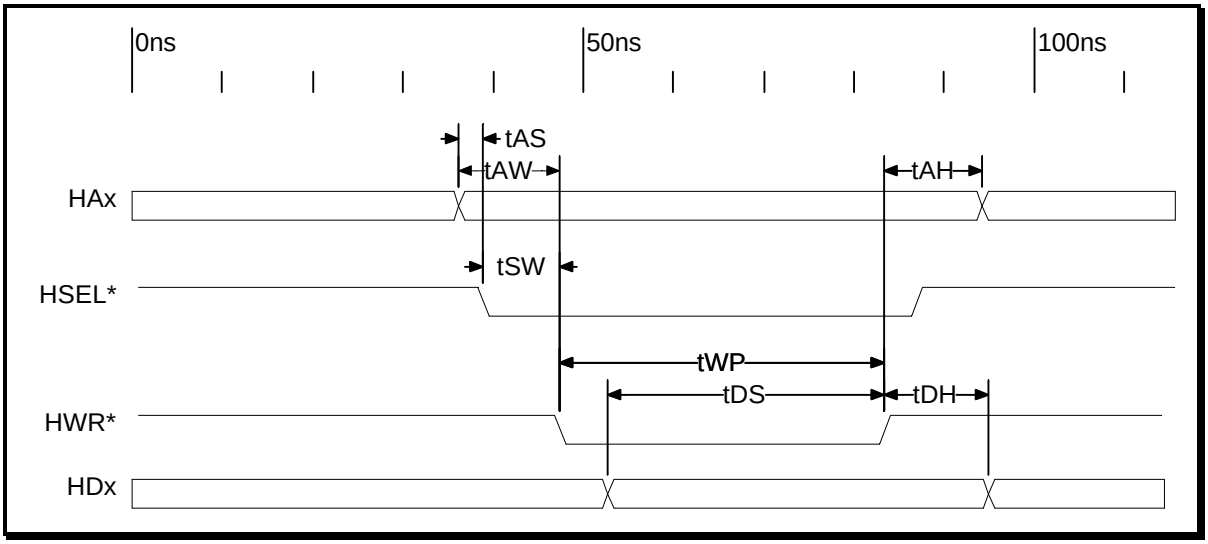

Figure 4-3 – MCI Write Timing Diagram

5. MECHANICAL SPECIFICATIONS

This section specifies the dimensional requirements, pinout, and recommended connectors for SHARCPAC modules and carrier boards.

5.1 DIMENSIONS

5.1.1 Module Dimensions

Figure 5-1 shows the dimensions for a SHARCPAC module. It shows the bottom side of the module (the side that faces the carrier board) and the mating connectors. The holes located at the corners are for mounting purposes only and have no electrical connection.

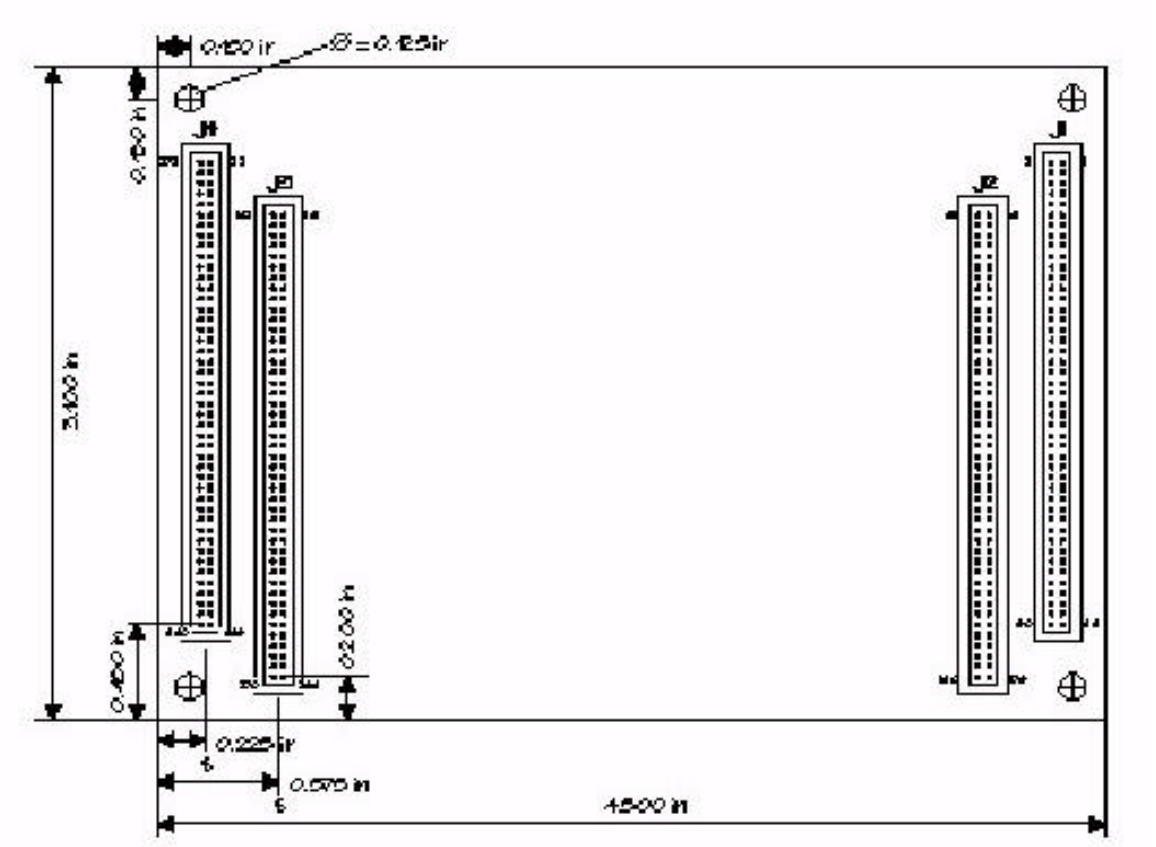

Figure 5-1 – SHARCPAC Module Dimensions, Bottom View

5.1.2 Module Site Dimensions

Figure 5-2 shows the dimensions for a SHARCPAC site on a carrier board. As stated above, the holes located at the corners are for mounting purposes only and have no electrical connection.

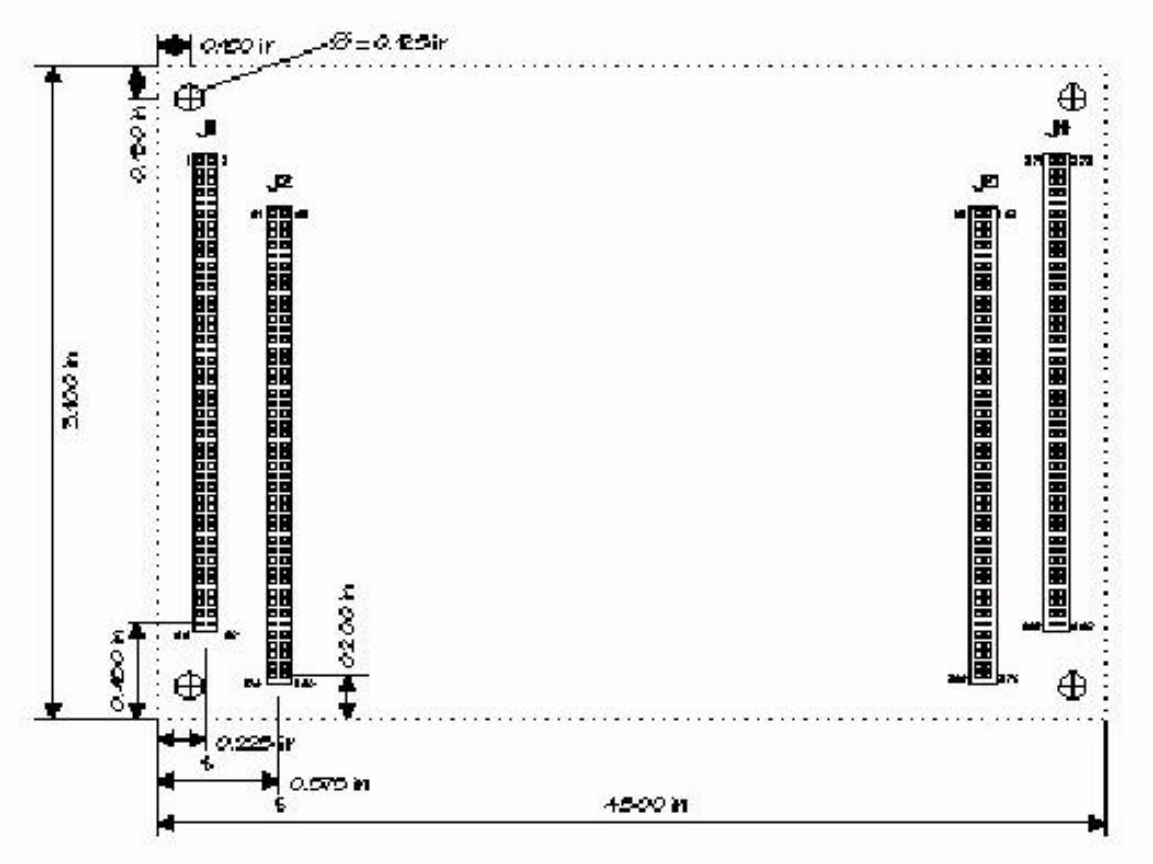

Figure 5-2 – SHARCPAC Carrier Site Dimensions, Top View

5.1.3 Module Site Spacing

Specifications are being considered for a double-wide module that spans two module sites. Contact the publisher of this document for the latest information regarding module site spacing.

5.1.4 Mating Dimensions

Figure 5-3 shows the side view of a SHARCPAC module mounted on a carrier board. The connectors on the carrier board have a fixed height; the connectors on the SHARCPAC module are available in multiple heights. Since components may be placed in the area below the SHARCPAC module, the module designer should chose the appropriate connector height to allow for adequate clearance for components installed on the bottom side of the module.

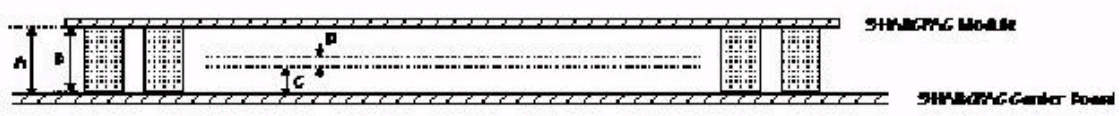

Figure 5-3 – Mated SHARCPAC Dimensions, Side View

Table 5-1 – Mated SHARCPAC Dimensions

Label	Description	Dimension
A	Module clearance	B + 0.025 in.
B	Module connector height	Available heights (in.): 0.225, 0.295, 0.365, 0.440
C	Maximum component height on carrier board	0.165 in.
D	Minimum clearance between components on module and components on carrier board	0.050 in.

5.2 RECOMMENDED CONNECTOR

Table 5-2 lists the connectors that should be used on the SHARCPAC module and carrier board. The connectors that mount on the carrier board are available in one height. The connectors that mount on the SHARCPAC module are available in various heights to accommodate components that are installed on the bottom side of the module.

Table 5-2 – Recommended Connectors

Location	Type	Manufacturer	Height (in.)	Part Number
Carrier Board (receptacle)	Surface Mount	Samtec	—	SFM-145-L2-S-D-LC
SHARCPAC Module (pin)	Surface Mount	Samtec	0.225	TFM-145-02-S-D-LC
			0.295	TFM-145-12-S-D-LC
			0.365	TFM-145-22-S-D-LC
			0.435	TFM-145-32-S-D-LC

5.3 PINOUT

The SHARCPAC module's 360 signals are implemented with four 90-pin connectors referenced by the names J1 - J4. The pins are numbered sequentially: J1 contains pins numbered 1-90, J2 contains the pins numbered 91-180, J3 contains pins numbered 181-270, and J4 contains the pins numbered 271-360. The following sections list the mapping between the signal names and the pin numbers alphabetically and then numerically. An asterisk (*) following a signal name indicates that the signal is active low.

5.3.1 Alphabetical List

PIN	NAME
306	ACK
99	ADDR00
100	ADDR01
101	ADDR02
102	ADDR03
103	ADDR04
104	ADDR05
105	ADDR06
106	ADDR07
108	ADDR08
109	ADDR09
110	ADDR10
111	ADDR11
112	ADDR12
113	ADDR13
114	ADDR14
115	ADDR15
117	ADDR16
118	ADDR17
119	ADDR18
120	ADDR19
121	ADDR20
122	ADDR21
123	ADDR22
124	ADDR23
126	ADDR24
127	ADDR25
128	ADDR26
129	ADDR27
130	ADDR28
131	ADDR29
132	ADDR30
133	ADDR31
299	ADRCLK
210	B0
223	B1
349	BMS*
217	BR1*
218	BR2*
307	BR3*
308	BR4*
215	BR5*
216	BR6*
222	CLKINA
135	CLKINB

PIN	NAME
294	CLKINC
171	CPA*
50	CS0*
303	CS1*
84	CS2*
304	CS3*
51	CS4*
52	CS5*
226	DATA00
227	DATA01
228	DATA02
229	DATA03
230	DATA04
231	DATA05
232	DATA06
233	DATA07
235	DATA08
236	DATA09
237	DATA10
238	DATA11
239	DATA12
240	DATA13
241	DATA14
242	DATA15
244	DATA16
245	DATA17
246	DATA18
247	DATA19
248	DATA20
249	DATA21
250	DATA22
251	DATA23
253	DATA24
254	DATA25
255	DATA26
256	DATA27
257	DATA28
258	DATA29
259	DATA30
260	DATA31
262	DATA32
263	DATA33
264	DATA34
265	DATA35
266	DATA36

PIN	NAME
267	DATA37
268	DATA38
269	DATA39
359	DATA40
358	DATA41
357	DATA42
356	DATA43
355	DATA44
354	DATA45
353	DATA46
352	DATA47
346	DMAG*
81	DMAR*
96	EMU*
8	FLAG0
30	FLAG1
287	FLAG2
286	FLAG3
139	FLAG4
138	FLAG5
311	FLAG6
310	FLAG7
7	GND
29	GND
38	GND
45	GND
48	GND
71	GND
76	GND
83	GND
116	GND
136	GND
156	GND
163	GND
178	GND
187	GND
205	GND
220	GND
224	GND
234	GND
252	GND
261	GND
277	GND
293	GND
298	GND

PIN	NAME
300	GND
309	GND
314	GND
328	GND
343	GND
345	GND
347	GND
348	GND
360	GND
22	GND
53	GND
134	GND
149	GND
180	GND
195	GND
243	GND
270	GND
285	GND
290	GND
329	GND
350	GND
198	HA0
199	HA1
200	HA2
201	HA3
211	HBG*
179	HBR*
63	HD0
64	HD1
65	HD2
66	HD3
67	HD4
68	HD5
69	HD6
70	HD7
54	HPROG0
55	HPROG1
56	HPROG2
57	HPROG3
58	HPROG4
59	HPROG5
60	HPROG6
61	HPROG7
203	HRD*
204	HSEL*

PIN	NAME
202	HWR*
97	ICSA*
289	IRQ0
288	IRQ1
197	IRQ2
196	IRQ3
46	IRQ4
47	IRQ5
312	IRQ6
313	IRQ7
9	L00ACK
10	L00CLK
11	L00DAT0
12	L00DAT1
13	L00DAT2
14	L00DAT3
192	L01ACK
191	L01CLK
280	L01DAT0
279	L01DAT1
190	L01DAT2
189	L01DAT3
157	L02ACK
158	L02CLK
159	L02DAT0
160	L02DAT1
161	L02DAT2
162	L02DAT3
327	L03ACK
326	L03CLK
325	L03DAT0
324	L03DAT1
323	L03DAT2
322	L03DAT3
23	L04ACK
24	L04CLK
25	L04DAT0
26	L04DAT1
27	L04DAT2
28	L04DAT3
276	L05ACK
275	L05CLK
186	L05DAT0
185	L05DAT1
274	L05DAT2

PIN	NAME
273	L05DAT3
164	L06ACK
165	L06CLK
166	L06DAT0
167	L06DAT1
168	L06DAT2
169	L06DAT3
320	L07ACK
319	L07CLK
318	L07DAT0
317	L07DAT1
316	L07DAT2
315	L07DAT3
16	L08ACK
17	L08CLK
18	L08DAT0
19	L08DAT1
20	L08DAT2
21	L08DAT3
184	L09ACK
183	L09CLK
272	L09DAT0
271	L09DAT1
182	L09DAT2
181	L09DAT3
150	L10ACK
151	L10CLK
152	L10DAT0
153	L10DAT1
154	L10DAT2
155	L10DAT3
335	L11ACK
334	L11CLK
333	L11DAT0
332	L11DAT1
331	L11DAT2
330	L11DAT3
6	L12ACK
5	L12CLK
4	L12DAT0
3	L12DAT1
2	L12DAT2
1	L12DAT3
284	L13ACK
283	L13CLK

PIN	NAME
194	L13DAT0
193	L13DAT1
282	L13DAT2
281	L13DAT3
143	L14ACK
144	L14CLK
145	L14DAT0
146	L14DAT1
147	L14DAT2
148	L14DAT3
342	L15ACK
341	L15CLK
340	L15DAT0
339	L15DAT1
338	L15DAT2
337	L15DAT3
140	MR*
41	MS0*
42	MS1*
43	MS2*
44	MS3*
305	PAGE
214	RD*
212	REDY
219	RESERVED
208	RESERVED
291	RESERVED
141	RPBA
39	SBTS
221	SENSE*
33	SP0DR
36	SP0DT
32	SP0RCLK
31	SP0RFS
35	SP0TCLK
34	SP0TFS
206	SP1DR
297	SP1DT
302	SP1RCLK
301	SP1RFS
296	SP1TCLK
207	SP1TFS
174	SP2DR
177	SP2DT
173	SP2RCLK

PIN	NAME
172	SP2RFS
176	SP2TCLK
175	SP2TFS
87	SP3DR
90	SP3DT
86	SP3RCLK
85	SP3RFS
89	SP3TCLK
88	SP3TFS
40	SW*
91	TCK
93	TDI
95	TDO
137	TIMEXP
92	TMS*
94	TRST*
72	User Defined
73	User Defined
74	User Defined
75	User Defined
77	User Defined
78	User Defined
79	User Defined
80	User Defined
15	VDD
37	VDD
82	VDD
98	VDD
107	VDD
170	VDD
188	VDD
209	VDD
278	VDD
292	VDD
295	VDD
321	VDD
351	VDD
49	VDD
62	VDD
125	VDD
142	VDD
225	VDD
336	VDD
344	VDD
213	WR*

5.3.2 Numerical List

J1

Pin	Name	Pin	Name
1	L12DAT3	2	L12DAT2
3	L12DAT1	4	L12DAT0
5	L12CLK	6	L12ACK
7	GND	8	FLAG0
9	L00ACK	10	L00CLK
11	L00DAT0	12	L00DAT1
13	L00DAT2	14	L00DAT3
15	VDD	16	L08ACK
17	L08CLK	18	L08DAT0
19	L08DAT1	20	L08DAT2
21	L08DAT3	22	GND
23	L04ACK	24	L04CLK
25	L04DAT0	26	L04DAT1
27	L04DAT2	28	L04DAT3
29	GND	30	FLAG1
31	SP0RFS	32	SP0RCLK
33	SP0DR	34	SP0TFS
35	SP0TCLK	36	SP0DT
37	VDD	38	GND
39	SBTS	40	SW*
41	MS0*	42	MS1*
43	MS2*	44	MS3*
45	GND	46	IRQ4
47	IRQ5	48	GND
49	VDD	50	CS0*
51	CS4*	52	CS5*
53	GND	54	HPROG0
55	HPROG1	56	HPROG2
57	HPROG3	58	HPROG4
59	HPROG5	60	HPROG6
61	HPROG7	62	VDD
63	HD0	64	HD1
65	HD2	66	HD3
67	HD4	68	HD5
69	HD6	70	HD7
71	GND	72	User Defined
73	User Defined	74	User Defined
75	User Defined	76	GND
77	User Defined	78	User Defined
79	User Defined	80	User Defined
81	DMAR*	82	VDD
83	GND	84	CS2*
85	SP3RFS	86	SP3RCLK
87	SP3DR	88	SP3TFS
89	SP3TCLK	90	SP3DT

J2

Pin	Name	Pin	Name
91	TCK	92	TMS*
93	TDI	94	TRST*
95	TDO	96	EMU*
97	ICSA*	98	VDD
99	ADDR00	100	ADDR01
101	ADDR02	102	ADDR03
103	ADDR04	104	ADDR05
105	ADDR06	106	ADDR07
107	VDD	108	ADDR08
109	ADDR09	110	ADDR10
111	ADDR11	112	ADDR12
113	ADDR13	114	ADDR14
115	ADDR15	116	GND
117	ADDR16	118	ADDR17
119	ADDR18	120	ADDR19
121	ADDR20	122	ADDR21
123	ADDR22	124	ADDR23
125	VDD	126	ADDR24
127	ADDR25	128	ADDR26
129	ADDR27	130	ADDR28
131	ADDR29	132	ADDR30
133	ADDR31	134	GND
135	CLKINB	136	GND
137	TIMEXP	138	FLAG5
139	FLAG4	140	MR*
141	RPBA	142	VDD
143	L14ACK	144	L14CLK
145	L14DAT0	146	L14DAT1
147	L14DAT2	148	L14DAT3
149	GND	150	L10ACK
151	L10CLK	152	L10DAT0
153	L10DAT1	154	L10DAT2
155	L10DAT3	156	GND
157	L02ACK	158	L02CLK
159	L02DAT0	160	L02DAT1
161	L02DAT2	162	L02DAT3
163	GND	164	L06ACK
165	L06CLK	166	L06DAT0
167	L06DAT1	168	L06DAT2
169	L06DAT3	170	VDD
171	CPA*	172	SP2RFS
173	SP2RCLK	174	SP2DR
175	SP2TFS	176	SP2TCLK
177	SP2DT	178	GND
179	HBR*	180	GND

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Pin	Name	Pin	Name
181	L09DAT3	182	L09DAT2
183	L09CLK	184	L09ACK
185	L05DAT1	186	L05DAT0
187	GND	188	VDD
189	L01DAT3	190	L01DAT2
191	L01CLK	192	L01ACK
193	L13DAT1	194	L13DAT0
195	GND	196	IRQ3
197	IRQ2	198	HA0
199	HA1	200	HA2
201	HA3	202	HWR*
203	HRD*	204	HSEL*
205	GND	206	SP1DR
207	SP1TFS	208	RESERVED
209	VDD	210	B0
211	HBG*	212	REDY
213	WR*	214	RD*
215	BR5*	216	BR6*
217	BR1*	218	BR2*
219	RESERVED	220	GND
221	SENSE*	222	CLKINA
223	B1	224	GND
225	VDD	226	DATA00
227	DATA01	228	DATA02
229	DATA03	230	DATA04
231	DATA05	232	DATA06
233	DATA07	234	GND
235	DATA08	236	DATA09
237	DATA10	238	DATA11
239	DATA12	240	DATA13
241	DATA14	242	DATA15
243	GND	244	DATA16
245	DATA17	246	DATA18
247	DATA19	248	DATA20
249	DATA21	250	DATA22
251	DATA23	252	GND
253	DATA24	254	DATA25
255	DATA26	256	DATA27
257	DATA28	258	DATA29
259	DATA30	260	DATA31
261	GND	262	DATA32
263	DATA33	264	DATA34
265	DATA35	266	DATA36
267	DATA37	268	DATA38
269	DATA39	270	GND

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Pin	Name	Pin	Name
271	L09DAT1	272	L09DAT0
273	L05DAT3	274	L05DAT2
275	L05CLK	276	L05ACK
277	GND	278	VDD
279	L01DAT1	280	L01DAT0
281	L13DAT3	282	L13DAT2
283	L13CLK	284	L13ACK
285	GND	286	FLAG3
287	FLAG2	288	IRQ1
289	IRQ0	290	GND
291	RESERVED	292	VDD
293	GND	294	CLKINC
295	VDD	296	SP1TCLK
297	SP1DT	298	GND
299	ADRCLK	300	GND
301	SP1RFS	302	SP1RCLK
303	CS1*	304	CS3*
305	PAGE	306	ACK
307	BR3*	308	BR4*
309	GND	310	FLAG7
311	FLAG6	312	IRQ6
313	IRQ7	314	GND
315	L07DAT3	316	L07DAT2
317	L07DAT1	318	L07DAT0
319	L07CLK	320	L07ACK
321	VDD	322	L03DAT3
323	L03DAT2	324	L03DAT1
325	L03DAT0	326	L03CLK
327	L03ACK	328	GND
329	GND	330	L11DAT3
331	L11DAT2	332	L11DAT1
333	L11DAT0	334	L11CLK
335	L11ACK	336	VDD
337	L15DAT3	338	L15DAT2
339	L15DAT1	340	L15DAT0
341	L15CLK	342	L15ACK
343	GND	344	VDD
345	GND	346	DMAG*
347	GND	348	GND
349	BMS*	350	GND
351	VDD	352	DATA47
353	DATA46	354	DATA45
355	DATA44	356	DATA43
357	DATA42	358	DATA41
359	DATA40	360	GND

6. LIST OF MANUFACTURERS

The following is a complete list of third-party manufacturers that provide components and services relevant to the SHARCPAC module.

Analog Devices
One Technology Way
PO Box 9106
Norwood, MA 02062-9106
(617) 329-4700

For Vendor Code information only, contact:

Len May
(617) 461-4308
E-mail: len.may@analog.com

Analog Devices manufactures the ADSP-2106x SHARC processor and maintains the list of unique SHARCPAC manufacturer Vendor Codes.

National Semiconductor
2900 Semiconductor Drive
PO Box 58090
Santa Clara, CA 95052-8090
(408) 721-5000

National Semiconductor manufactures the NM93C42AL serial EEPROM.

SAMTEC Incorporated
PO Box 1147
New Albany, IN 47151-1147
(800) SAMTEC-9 (USA & Canada)
(812) 944-6733

SAMTEC manufactures the connectors used to bring the external signals of the SHARCPAC module to the host system board.

7. SPECIFICATION REVISION HISTORY

Below is a complete revision history of this specification. Manufacturers of SHARCPAC modules and host systems with SHARCPAC sites should reference the revision of this specification to which their product adheres to indicate a level of compliance.

Date	Revision	Comments
2-94	1.0	First release.
2-95	1.1	Improved clock distribution scheme, adding 2 CLKIN signals.
2-96	1.2	First public release. Added ADRCLK, BMS, and DMAR/DMAG signals.